Study on Geometrical Variation Effects to the Performance of Silicon Split Gate Flash Memory with Tapered Floating Gate Structure

Muhammad Amin Sulthoni[a, b, *], Akhmadi Surawijaya[a, b]

[a]*Microelectronics Center, Institut Teknologi Bandung, Jalan Ganesha 10, Bandung, Indonesia*
[b]*School of Electrical Engineering and Informatics, Institut Teknologi Bandung, Jalan Ganesha 10, Bandung, Indonesia*
**Corresponding Autor's Email: mamiens@stei.itb.ac.id*

Abstract: We present a study on the effect of geometrical variation on electrical performance of a silicon split gate flash memory with tapered floating gate structure. Numerical simulation study is performed using Sentaurus Synopsis. Fabrication of flash memory structure with various geometry is first simulated and resulting structures then simulated for I-V characteristics during program-erase cycles. Hot electron tunnelling mechanism is simulated during program cycle while Fowler Nordheim tunneling is used in erase cycle. The result shows that thinner floating gate and larger ratio of side gate's lenght over floating gate's lenght resulted in larger threshold voltage shifting, while optimization between tunnelling oxide thickness and device structure is required to achieve larger threshold shifting of the flash memory.

Keywords: *Silicon flash memory, numerical study, simulation, electron tunneling, charge storage*

INTRODUCTION

This paper describes the results of a study of the change in the characteristics of a split gate flash memory device with a tapered floating gate structure against a variety of structural geometries, performed using numerical simulation approach. Fabrication process that resulted in the structure is first simulated with variation in tunnelling oxide thickness, floating gate thickness, as well as the ratio of floating gate length to side gate length. The resulting device structure is then simulated for its I-V characteristics to examine the effect of structure geometrical variation. The result shows that these geometrical variations affect the shifting of threshold voltage between program and erase cycle of the flash memory.

MATERIALS AND METHODS

Fabrication process of silicon split gate flash memory structure is first simulated using Sentaurus Synopsis process while varying the thickness of floating gate and tunneling oxide located beneath, and the ratio between side gate's length and floating gate's length (L_{SG}/L_{FG}). Standard CMOS fabrication process is used to create the split gate flash memory while some modification is added to create tapered floating gate structure. The resulting split gate structures are then simulated for program-erase cycles' I-V characteristics using Sentaurus Synopsys device. Hot electron tunneling mechanism is used in program cycle while the Fowler Nordheim tunneling mechanism is used in erase cycle. Trapped electron densities inside floating gate were also examined to analyze simulation result.

RESULTS AND DISCUSSION

Left graphic of Fig. 1 shows a typical case of threshold voltage shifting between program (right curve) and erase (left curve) process cycle, in this case are for various ratio of L_{SG}/L_{FG}. The result suggests that higher ratio that means shorter floating gate will introduce larger threshold voltage shifting [3, 4]. Since program cycle used in the simulation is the same in all conditions, we assume that number of trapped electron in floating gate is slightly similar. However trapped electron density is larger for

smaller floating gate as depicted in the right side graphic of Fig.1, so that change in electric field distribution affected by the trapped electron is stronger which resulted in larger threshold voltage shifting. A thinner floating gate will result in higher trapped electron density and provide greater threshold voltage shifting.

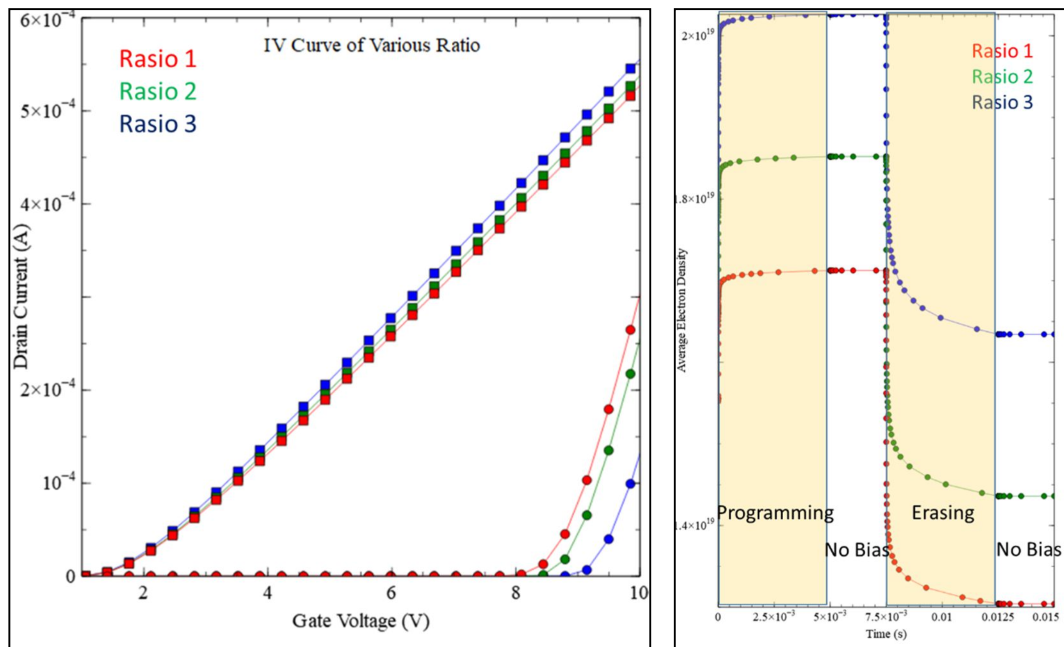

Fig. 1. Left: Threshold voltage shifting for various ratio of L_{SG}/L_{FG} (0,37; 0,50; 0,65). Right: Trapped electron density at various L_{SG}/L_{FG} [1, 2].

CONCLUSIONS

The simulation result shows that thinner floating gate and larger ratio of side gate's length over floating gate's length resulted in larger threshold voltage shifting, while optimization between tunnelling oxide thickness and device structure is required to achieve larger threshold shifting of the flash memory. Scaling attempt or redesigning of other split gate flash memory can be performed based on these results. However, the simulations are performed using standard parameters of the materials, processes, and mechanisms. Therefore, some tuning is required to get more accurate result.

ACKNOWLEDGMENT: The authors would like to express appreciation for the support of 2017 ITB-P3MI research project.

REFERENCES

[1] Kartiwa G.M., Hendrayana Y.H., Prihatiningrum N., Sulthoni M.A., Surawijaya A., Idris I. Effect of L_{SG}/L_{FG} Ratio Variation to the IV Curve of Split Gate 1st Generation Superflash. Proceeding of ISESD 2017, pp 264.

[2] Kartiwa G.M., Sulthoni M.A., Surawijaya A., and Idris I. Threshold Voltage Shift of the 1ST Gen Split-Gate SuperFlash Memory Cell with Various Geometry Variations. Submitted for publication.